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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,233	08/08/2001	Kerry Bernstein	BUR920010042	9886

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,233	BERNSTEIN ET AL.	
	Examin r	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final rejection

Response to the applicant's amendments

********Applicants argument with respect to original claims 1-32 filled in 08/31/04 have been fully considered but they are not persuasive. The examiner would like to point out that this action is made final (MPEP 706.07a).

Response to the applicants' argument

Response to Remark pages 11-17, the applicant argues that the prior arts do not show any latches or logic circuits (or stages) connected to power supplies. However, the flip-flops or logic circuits must be powered to work properly. This reasoning also means that at least one power supply must be present to power the flip-flops and logic circuits. The connection between a power supply and a flip-flop necessarily requires a medium for wiring between the connections and the wiring is analogous to the claimed power rails and the more flip-flops utilized in a circuit configuration, the more the numbers of wiring or power rails involved.

As for the argument that no power supplies are connected to the logic circuits or flip-flops in Tsukamoto et al's art, there is no logic circuit or flip-flop that operates with out power application from a common or multiple power supplies. Although the examiner strongly disagrees with the argument based on the fact that the power distribution block (19) supplies power directly or indirectly to the logic circuits, even with the absence of it, it is obvious that the prior art logic circuits cannot properly function with out being powered by power supply means.

As for the argument concerning clocks, it is clear from figure 3 of Rajassamy that the first clock (302) must be clocked by CK1N to accept input and it also requires another

clock to output the input. Second latch (306) follows the same behavior in relation to CK2N. Please not that said rail are considered to be equivalent to the power supply wires in the prior art and the examiner would like to point out that supplying power to multiple devices through a common rail is notoriously known in the art to minimize circuit density. Therefore, this action bases the reflection on this understanding point in view is how a memory devices use to receive power from a common rail and avoid circuit density proportional to the memory cells in a given array. In light of the responses above, the examiner believes that the prior art were properly applied.

As for claim 11, the prior art (Rajassamy) at least shows three stages of flip-flop circuit's configurations, first stage comprising (302, 304), the second stage comprising (306, 308) and the third stage comprising (310, 312) each have control clocks and power applications. Clearly the input/output relationship of the stages is cascaded similar to the claimed configuration. Although the prior art may have shown three stages for a particular application, it is clear that the stages can expand beyond three stages to multiple more depending on anticipated application. Therefore, number of stages are known variable in the art depending on the applications requirement. Further duplicating circuit configuration to expand the scope of a given circuit is not patentable by itself.

As for the number of power rails in the claimed invention, the concept is discussed in relation to claim 1. As for the argument in regards to claim 17, the device of the prior art is capable of functioning according to claimed methods by virtue of circuit and conceptual similarities. Therefore, in light of the above, the final rejection holds strong in view of the recited references.

1. Claims **1 to 32** remain pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims **1-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Radjassamy (U.S. PN: 6,331,800) in view of Tsukamoto et al. (U.S. PN: 5,930,269).

As per claims **1 and 6,** Radjassamy in figure 3 disclose or teach an integrated circuit comprising a first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308) for adjusting of clock edge rise/fall times between non-overlapping clock signals and thereby eliminate a race (see col. 1, lines 5-9). Further, Radjassamy teach a method of

increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy **do not explicitly** show or teach power (rails) applied separetly to each of the IC chips wherein each IC chips comprise latches and logic circuits. **However,** Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (IC11/IC12/IC1n, IC21/IC22/IC2n...) of a semiconductor integrated circuit device arranged in rows and columns on the burn-in board, and are electrically connected through contact pins and furthermore Power supply lines VCC1, VCC2 and VCCm (power rails) are respectively associated with the columns of products of semiconductor device and the products are powered with power potential Vcc and the ground potential supplied from the associated power supply lines VCC1 to VCCm (see col. 3, lines 55-67 and col. 4, lines 1-22). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsukamoto et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to diagnosis the

products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58).

As per claims **2 and 7,** Radjassamy in view of Tsukamoto et al. teach all the subject matter claimed in claims 1 and 6 including Radjassamy in figure 3 disclosed second latch (308) coupled to the second logic (circuit) (306) whereby the second latch and the second logic circuit coupled to the second clock (CK2N). Furthermore, Tsukamoto et al. in figure 5 teach plurality of voltage lines or rails connected to each of the board products (chips) separately (see VCC1, VCC2 ..).

As per claims **3-5 and 8-10,** Radjassamy in view of Tsukamoto et al. teach all the subject matter claimed in claims 1 and 6 including Tsukamoto et al. in figure 5 teach plurality of burn-in products whereby each of the products connected by separate scan clocks (SCN1, SCN2...) and voltage lines (VCC1, VCC2...).

As per claims **11-16,** Radjassamy substantially teach or disclose an integrated circuit comprising clocked logic gates a method for increasing the rise/fall of clock edges in an IC commencing with the identification (detecting) of a clock signal with a clock edge having a poor rise/fall time (see abstract and col. 3, lines 34-43). Further, Radjassamy in figure 3, disclose first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308). Furthermore, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the

identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy **do not explicitly** show or teach power (rails) applied separately to each of the IC chips wherein each IC chips comprise latches and logic circuits. **However,** Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (IC11/IC12/IC1n, IC21/IC22/IC2n...) of a semiconductor integrated circuit device arranged in rows and columns on the burn-in board, and are electrically connected through contact pins and furthermore Power supply lines VCC1, VCC2 and VCCm (power rails) are respectively associated with the columns of products of semiconductor device and the products are powered with power potential Vcc and the ground potential supplied from the associated power supply lines VCC1 to VCCm (see col. 3, lines 55-67 and col. 4, lines 1-22). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsukamoto et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58).

As per claims **17 and 22,** Radjassamy in view of Tsukamoto et al. teach or disclose all the subject matter claimed in claims 1 and 6, including Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Furthermore, Tsukamoto et al. teach a testing system selectively activates products of a semiconductor integrated circuit device mounted on a burn-in board and a power distributor incorporated in the testing system supplies electric power only to the activated products so that non-activated products do not affect the test data signals (see abstract).

As per claims **18-21 and 23-26,** Radjassamy in view of Tsukamoto et al. teach all the subject matter claimed in claims 1 and 6 including Radjassamy in figure 3 disclosed second latch (308) coupled to the second logic (circuit) (306) whereby the second latch and the second logic circuit coupled to the second clock (CK2N). Furthermore, Tsukamoto et al. in figure 5 teach plurality of voltage lines or rails connected to each of the board products (chips) separately (see VCC1, VCC2 ..).

As per claims **27-32,** Radjassamy in view of Tsukamoto et al. teach or disclose all the subject matter claimed in claim 11, including Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method

commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Furthermore, Tsukamoto et al. teach a testing system selectively activates products of a semiconductor integrated circuit device mounted on a burn-in board and a power distributor incorporated in the testing system supplies electric power only to the activated products so that non-activated products do not affect the test data signals (see abstract).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham
Esaw Abraham

Guy J. Lamarre
Primary Examiner